Docket No.: 50006-070

UTILITY PATENT APPLICATION UNDER 37 CFR 1.53(b)

Box PATENT APPLICATION
Assistant Commissioner for Patents
Washington, DC 20231
Sir:

Transmitted herewith for filing is the patent application of:

INVENTOR: Jiro MATSUFUSA, Tomoharu MAMETANI, Takeshi KISHIDA, Yoji NAKATA, Yukihiro NAGAI, Hiroaki NISHIMURA, Akinori KINUGASA, Shigenori KIDO
FOR: SEMICONDUCTOR DEVICE HAVING TEST MARK

Enclosed are:

- ☒ 17 pages of specification, claims, abstract.
- ☒ Declaration and Power of Attorney.
- ☒ Priority Claimed.
- ☒ Certified copy of Japanese Patent Application No. 2000-015760
- ☒ 10 sheets of formal drawing.
- ☒ An assignment of the invention to Mitsubishi Denki Kabushiki Kaisha and the assignment recordation fee.
- ☐ An associate power of attorney.
- ☐ A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27.
- ☒ Information Disclosure Statement, Form PTO-1449 and reference.
- ☒ Return Receipt Postcard
- ☒ Please note the **correct address** for the third inventor, Takeshi KISHIDA , is c/o LTEC CORPORATION, 4-42-8, Higashiarioka, Itami-shi, HYOGO 664-0845 JAPAN

The filing fee has been calculated as shown below:

	NO. OF CLAIMS		EXTRA CLAIMS	RATE	AMOUNT
Total Claims	8	-20	0	$18.00	$0.00
Independent Claims	1	-3	0	$78.00	$0.00
				Multiple Dependent Claim(s)	$0.00
				Basic Fee	$690.00
				Total of Above Calculations	$690.00
				Less ½ for Small Entity	$0.00
				Assignment & Recording Fee	$40.00
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Respectfully submitted,

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SEMICONDUCTOR DEVICE HAVING TEST MARK

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a semiconductor device having a test mark and, more particularly, to a semiconductor device in which an extension of a crack from the test mark is prevented.

Description of the Related Art

Referring to Fig. 13A, a semiconductor wafer 10 contains a plurality of block portions 11. In the process of fabricating semiconductor elements on the semiconductor wafer 10, each of the block portions 11 is exposed to light in one shot process.

Referring to Fig. 13B, which shows an enlarged block portion 11, a plurality of semiconductor chips 12 are fabricated in the block portion 11, and also dicing lines or tracks 13 along which the block portion 11 will be diced and separated into semiconductor chips 12 are formed between the semiconductor chips 12. Generally, a test mark (not shown) is formed in the dicing line 13, for example, for measuring a thickness of a deposited layer, determining overlay accuracy, or measuring a characteristic of a device.

Referring next to Fig. 14A, there is shown an enlarged plan view of a test mark fabricated in the dicing

line. Also, a cross sectional view along lines B-B in Fig. 14A is shown in Fig. 14B. As shown, a semiconductor substrate 21 bears a first insulating layer 22 made of tetraethyl orthosilicate including boron and phosphorus which has good characteristic of step coverage, referred to "BPTEOS layer" hereinafter, which in turn supports a second insulating layer 23 made of tetraethyl orthosilicate, referred to "TEOS layer" hereinafter. A recess or concave 24 for use as a test mark is formed in the TEOS and BPTEOS layers, 22 and 23, and terminated at the surface of the substrate 21 facing to the BPTEOS layer 22. When viewed from above, i.e., from the direction indicated by the arrow 29 in Fig. 14B, the recess 24 has a square in configuration defined by four vertical walls, and one side of the square recess 24 is about 10 to 100μm in length.

Disadvantageously, the BPTEOS layer 22 is melted or deformed in a heat treatment such as a sintering step, on the other hand, the TEOS layer 23 is scarcely deformed in the step. This results in that cracks 27 are formed in the BPTEOS layer 22 at the corner of the recess 24 near the TEOS layer 23 as shown in Fig. 14A. The cracks 27 extend outwardly and then destroy the semiconductor elements or another test marks (not shown) fabricated on the semiconductor substrate 21.

Particularly, the test mark has a large area in

horizontal cross section such as a square configuration of 100μm x 100μm or a rectangular configuration of 1μm x 100μm, for example, and has four corners. Therefore, stresses concentrate at these corners by the deformation of the BPTEOS layer 22, causing the formation of the cracks 27.

In order to prevent formation of the cracks 27, a structure shown in Figs. 15A and 15B has been proposed. In the structure, a metal layer 25 such as a capacitor lower electrode is formed on the BPTEOS 22 as a stop layer, thereby a recess 24 is formed only in the TEOS layer 23 above the metal layer 25.

However, for example, the thickness of the TEOS layer 23 can not be measured exactly by the use of the test mark. This is because the metal layer 25 is formed in the TEOS layer 23. Therefore, the test mark is prohibited from being used for the measurement of the thickness of the TEOS layer 23. Also, the presence of the metal layer 25 prevents the exact determination of overlay accuracy. Therefore, the mark is not used for determining overlay accuracy.

SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is to provide a semiconductor device having a test mark which prevents extension of a crack arisen at the corner of

a recess which is used as a test mark, thereby adverse affect to a semiconductor element by the crack is prevented.

To this end, the inventors of the present invention have made intensive research on this subject. As a result, the inventors have found that by forming a metal layer on the BPTEOS layer near the corners of the recess, thereby the extension of the cracks formed in the BPTEOS layer can be terminated by the metal layer.

That is, present invention provides a semiconductor device having a test mark. The device comprises a semiconductor substrate; a first TEOS layer formed on the semiconductor substrate; a second TEOS layer formed on the first TEOS layer and having a fluidity lower than that of the first TEOS layer at high or an elevated temperature; a recess formed in the first and second TEOS layers and terminated at the surface of the semiconductor substrate, wherein the horizontal cross section of the recess is substantially rectangular in configuration; and a metal layer formed between the first and second TEOS layers and opposing to the corner of the recess.

In the case that a crack is arisen in the first TEOS layer at the corner of recess by the deformation of the first TEOS layer, the extension of the crack can be terminated by the metal layer. Thereby, the destruction of a semiconductor element or another test mark, which is

caused by the extension of the crack, can be prevented.

The first TEOS layer may contain boron and/or phosphorus. Such a TEOS layer containing boron and/or phosphorus, which is referred as a BPTEOS layer, is easy to melt or deform, so that a crack is easy to arise.

Preferably, the metal layer is a square-shaped layer surrounding the recess. By use of such a metal layer, the extension of a crack can be terminated.

The metal layer may be an L-shaped layer surrounding the corner of the recess. This is because that most of the cracks are arisen at the corner of the recess and extend in a diagonal direction of the recess.

The metal layer may be a delta-shaped layer of which one side opposes to the corner of the recess. The extension of a crack can be terminated effectively by such a metal layer.

Also, a semiconductor device of the present invention may further comprise an outer metal layer formed outside of the metal layer so that the outer metal layer opposes to the corner of the recess through the metal layer.

A crack that extends through and outward the metal layer can be terminated by the outer metal layer.

Also, a semiconductor device of the present invention may further comprise a lower metal layer embedded in the first TEOS layer which extends between the top and

bottom surfaces each neighboring to the semiconductor substrate and the metal layer. The extension of a crack can be terminated effectively by such an embedded metal layer.

The lower metal layer may consist of a plurality of cylindrical metal layers.

As can be seen from above description, a crack extended from the corner of the recess for use as a test mark can be terminated by the metal layer which is formed around the recess. Thereby, a production yield of a semiconductor device having such a test mark can be increased.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A is a plan view of a semiconductor device having a test mark according to the present invention;

Fig. 1B is a cross sectional view of the semiconductor device along lines A-A in Fig. 1A;

Figs. 2A to 2C are a semiconductor device according to the present invention;

Figs. 3A to 3G are cross sectional views of a semiconductor device at different steps in its producing process according to the present invention;

Figs. 4 to 12 are a semiconductor device having another test mark according to this invention;

Fig. 13A is a plan view of a semiconductor wafer containing a plurality of semiconductor chips;

Fig. 13B is an enlarged plan view of the semiconductor chip of Fig. 13A;

Fig. 14A is a plan view of a conventional semiconductor device having a test mark;

Fig. 14B is a cross sectional view of the semiconductor device along lines B-B in Fig. 14A;

Fig. 15A is a plan view of a conventional semiconductor device having a test mark; and

Fig. 15B is a cross sectional view of the semiconductor device along lines C-C in Fig. 15A.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Fig. 1A, there is shown an enlarged partial plan view of the semiconductor device generally indicated by reference numeral 100. The semiconductor device is formed at its one surface with a dicing line 8 having a certain width, along which a grooving or dicing will be done.

Fig. 1B shows a cross sectional view of a part of the semiconductor device 100 along lines A-A in Fig. 1A. As can be seen from this drawing, the semiconductor device 100 includes a substrate 1 on which semiconductor elements (not shown) are integrated. For clarify, the semiconductor

elements are eliminated from the drawings. The semiconductor substrate 1 bears a first insulating layer 2 made of tetraethyl orthoslicate including boron and phosphorus, referred to as "BPTEOS layer" hereinafter, which in turn supports a second insulating layer 3 made of tetraethyl orthoslicate, referred to as "TEOS layer" hereinafter.

Within the dicing line 8, a recess or concave 4 for use as a test mark is formed in the first and second layers, BPTEOS and TEOS layers 2 and 3, which terminates at the surface of the substrate 1 facing to the BPTEOS layer 2. When viewed from above, i.e., from the direction indicated by the arrow 9 in Fig. 1B, the recess 9 has a square in configuration defined by four vertical walls. It may be envisioned that the recess 4 is a rectangular in configuration.

The BPTEOS layer 2 includes a first metal layer 5 leaving a certain space from and running around the recess 4. In this embodiment, the first layer extends between the top and bottom surfaces each neighboring to the TEOS layer 3 and the substrate 1. The formation of this metal layer 5 will be described later. Also, the TEOS layer 3 includes a second metal layer 6 embedded in its bottom surface facing to the BPTEOS layer 2. The second metal layer 6 runs along the first metal layer 5. As can be seen from Fig. 1B, the

second metal layer 6 has s width greater than that of the first metal layer 5.

It should be noted that the BPTEOS layer 2 is made of material having a specific melting point which is less than a temperature in which the semiconductor device 100, after it is mounted with various parts, is heat treated to fuse electrical connecting parts such as solder bumps. In contrast, the TEOS layer 3 is made of material having a specific melting point greater than the fusing temperature. As a result, in the heat treatment, the BPTEOP layer 2 melts or softens. The TEOS layer 3, on the other hand, does not melt or soften in the heat treatment. This may result in a crack 7 at each corner of the square recess 4 of the BPTEOS layer 2.

This crack 7 tends to extend in a diagonal direction as shown in Fig 1A, but it terminates at the metal layer 6 and will never extend beyond the metal layer 6. This is advantageous that the crack 7 would never provided adverse affect to the semiconductor elements or other recesses (not shown) disposed outside the metal layer 6.

Fig. 2A is a partial plan view of the semiconductor device 100 shown in Fig 1A. In Fig. 2A, the TEOS layer 3 is eliminated from the drawing. Fig. 2B is a cross sectional view of the semiconductor device 100 along

lines 2B-2B in Fig 2A, and Fig. 2C is a cross sectional view of the semiconductor device 100 along lines 2C-2C in Fig 2A. In Figs. 2B and 2C, the substrate 1 is eliminated from the drawings. As shown in Figs. 2A to 2C, the first metal layer 5 is plate-shaped and extends through the BPTEOS layer 2 between the substrate 1 and the second metal layer 6.

Referring next to the Figs. 3A to 3G, the method for fabricating the semiconductor device having a test mark will be described.

In this process, as shown in Fig. 3A, a BPTEOS layer 2 is formed on a semiconductor substrate 1 as a first insulating layer. Also, as shown in Fig. 3B, by use of conventional photolithography and etching techniques, grooves 2' are formed in the BPTEOS layer 2.

Subsequently, as shown in Fig. 3C, a first metal material layer 5' is deposited on the entire surface of the BPTEOS layer 2 so as to embed the grooves 2'. Then, by use of conventional CMP or etch back techniques, the first metal material layer 5' is polished so as to remain in the grooves 2'. The remained first metal material layers 5' are used as metal layers 5 as shown in Fig. 3D.

Then, as shown in Fig. 3E, a second metal material layer (not shown) is deposited on the BPTEOS layer 2 and the metal layers 5, in turn, it is patterned to form

a second metal layer 6. The second metal layer 6 runs along and covers the first metal layers 5 continuously as shown in Fig. 3E.

Finally, as shown in Fig. 3F, a TEOS layer is deposited on the BPTEOS layer 2 and the second metal layer 6. Also, as shown in Fig. 3G, the TEOS and PBTEOS layers, 3 and 2, are etched, so that a recess or concave 4 is formed which is used as a test mark. Then a semiconductor device 100 according to this embodiment is accomplished.

It is noted that preferably the first and second metal layers, 5 and 6, may be made from aluminum, copper or aluminum silicate.

In Fig. 4A, there is shown a partial plan view of a semiconductor device of another variation of this embodiment, in which the TEOS layer 3 is eliminated from the drawing. Fig. 4B is a cross sectional view of the semiconductor device along lines 4B-4B in Fig 4A, and Fig. 4C is a cross sectional view of the semiconductor device along lines 4C-4C in Fig 4A. In Figs. 4B and 4C, the substrate 1 is eliminated from the drawings.

As illustrated in these drawings, a plurality of the metal layers, each of which is cylindrical and extends between the top and the bottom surfaces of the BPTEOS layer 2, may be used as a first metal layers 5.

Fig. 5A is a partial plan view of a semiconductor

device of another variation of this embodiment, in which the TEOS layer 3 is eliminated from the drawing. Fig. 5B is a cross sectional view of the semiconductor device along lines 5B-5B in Fig 5A, and Fig. 5C is a cross sectional view of the semiconductor device along lines 5C-5C in Fig 5A. In Figs. 5B and 5C, the substrate 1 is eliminated from the drawings.

As illustrated in these drawings, no first metal layer is formed beneath the second metal layer 6. That is, only the second metal layer 6 terminates the extension of the crack from the corner of the test mark (not shown).

In the producing process described above, the first and second metal layers, 5 and 6, are formed in the separate steps, however, these layers may be formed in one step. That is, after the first metal material layer 5' is deposited on the BPTEOS layer 2 as shown in Fig. 3C, the first and second metal layers, 5 and 6, are formed simultaneously by use of conventional photolithography and etching techniques. This result in that the first and second metal layers, 5 and 6, are formed from the first metal material layer 5' as shown in Figs. 6A and 6B, which are cross sectional views of a semiconductor device.

Referring to Figs. 7 to 12, preferred formations of the second metal layer 6 on the BPTEOS layer 2 are shown. The Figs. 7 to 12 are partial top views of a semiconductor

device 100 having a test mark 4. For clarify, TEOS layers are eliminated from these drawings.

As shown in Fig. 7, the second metal layer 6 may be formed to surround and leave a certain space from the recess 4, so that the second metal layer 6 is a square-shaped layer. By surrounding the recess 4 by the second metal layer 6, extension of a crack from the corner of the recess 4 can be terminated by the second metal layer 6.

Also, as shown in Fig. 8, each of the second metal layer 16 may be an L-shaped layer, which surrounds the corner of the recess 4. As described above, at the corner of the recess 4, a stress in concentrated, causing the formation of the crack, and the crack tends to extend in a diagonal direction of the recess 4. Therefore, the second metal layer 16, which is opposed to the corner of the recess 4, can terminate the extension of the crack.

Also, as shown in Fig. 9, each of the second metal layer 26 may be a delta-shaped layer of which one side opposes to the corner of the recess 4. Most of the cracks are generated at the corner of the recess 4, therefore the delta-shaped layer 26 can terminate the extension of the crack.

Further, as shown in Figs. 10 to 12, another metal layer may surround the metal layer described above. That is, referring to Fig. 10, the L-shaped metal layer 16

is formed to be opposed to the each corner of the square-shaped metal layer 6. Also, referring in Fig. 11, the delta-shaped metal layer 26 is formed to be opposed to the each corner of the square-shaped metal layer 6. Further, referring to Fig. 12, the delta-shaped metal layer 26 is formed to be opposed to the each corner of the L-shaped metal layer 16 which is opposed to the corner of the recess 4.

By forming inner and outer metal layers described above, in the case that the crack expands through and outward the inner metal layer, the expansion of the crack can be terminated by the outer metal layer.

It is noted that a first metal layer 5 may be formed beneath these metal layers 6, 16 and 26.

WHAT IS CLAIMED IS:

1. A semiconductor device having a test mark comprising:

a semiconductor substrate;

a first TEOS layer formed on said semiconductor substrate;

a second TEOS layer formed on said first TEOS layer and having a lower fluidity than that of said first TEOS layer at an elevated temperature;

a recess formed in said first and second TEOS layers and exposing the surface of said semiconductor substrate, wherein the horizontal cross section of said recess is substantially rectangular in configuration; and

a metal layer formed on said first TEOS layer and opposing to the corner of said recess.

2. A semiconductor device according to claim 1, wherein said first TEOS layer contains boron and/or phosphorus.

3. A semiconductor device according to claim 1, wherein said metal layer is a square-shaped layer surrounding said recess.

4. A semiconductor device according to claim 1, wherein said metal layer is an L-shaped layer surrounding the corner of said recess.

5. A semiconductor device according to claim 1, wherein said metal layer is a delta-shaped layer of which one side opposes to the corner of said recess.

6. A semiconductor device according to claim 1, further comprising an outer metal layer formed outside of said metal layer so that said outer metal layer opposes to the corner of said recess through said metal layer.

7. A semiconductor device according to claim 1, wherein a lower metal layer is embedded in said first TEOS layer which extends between the top and bottom surfaces each neighboring to said semiconductor substrate and said metal layer.

8. A semiconductor device according to claim 7, wherein said lower metal layer consists of a plurality of cylindrical metal layers.

ABSTRACT OF THE DISCLOSURE

A semiconductor device having a test mark comprising: a semiconductor substrate; a first TEOS layer formed on the semiconductor substrate; a second TEOS layer formed on the first TEOS layer and having a fluidity lower than that of the first TEOS layer at an elevated temperature; a recess formed in the first and second TEOS layers and exposing the surface of the semiconductor substrate, wherein the horizontal cross section of the recess is substantially rectangular in configuration; and a metal layer formed between the first and second TEOS layers and opposing to the corner of the recess.

Fig. 1A

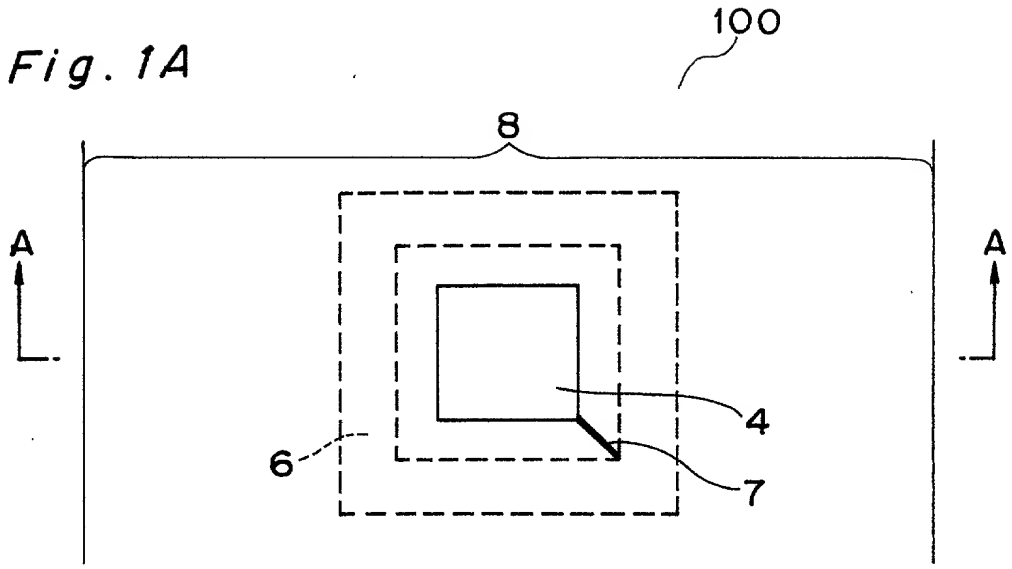


Fig. 1B

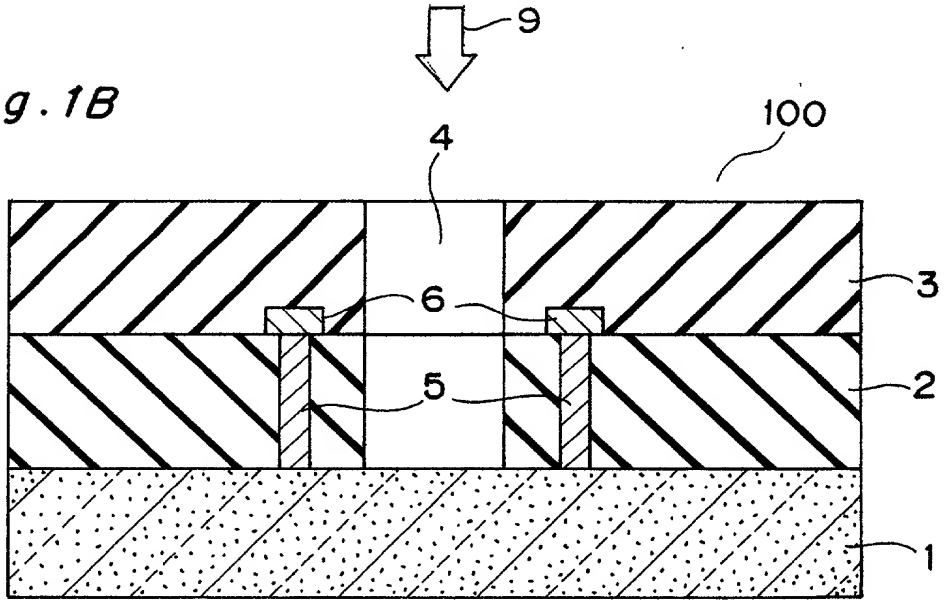


Fig.2A

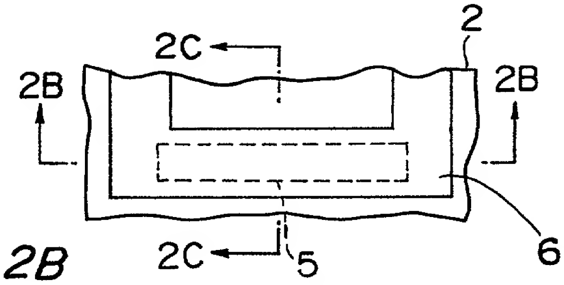


Fig.2B

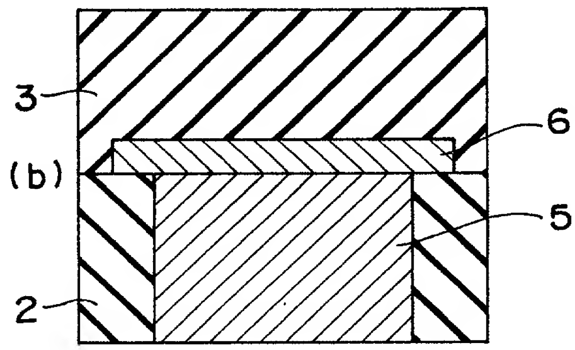


Fig.2C

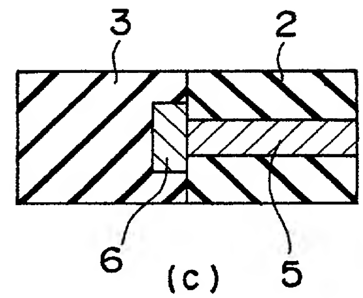


Fig.4A

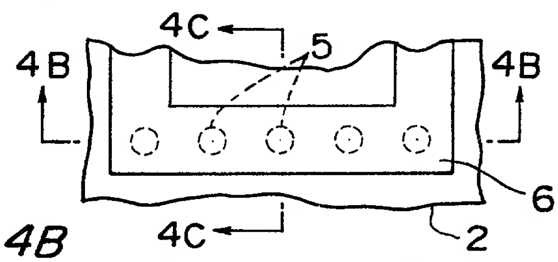


Fig.4B

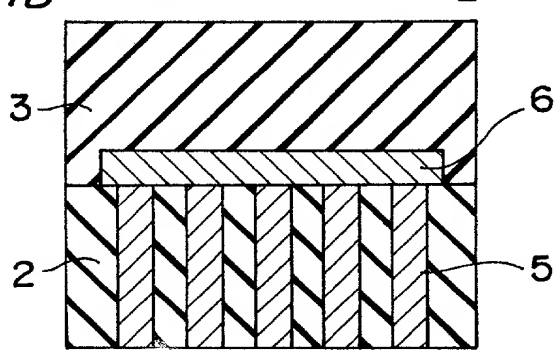


Fig.4C

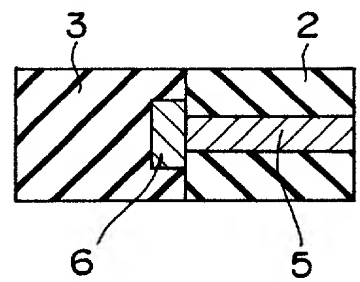


Fig.3A

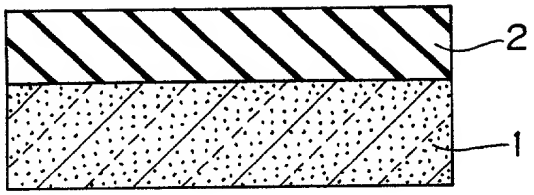


Fig.3B

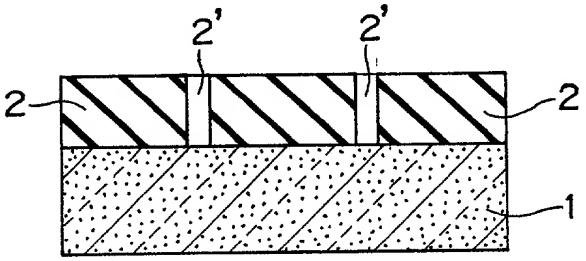


Fig.3C

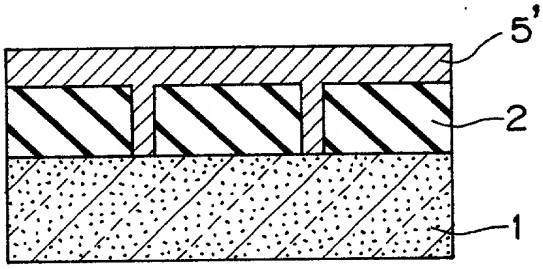


Fig.3D

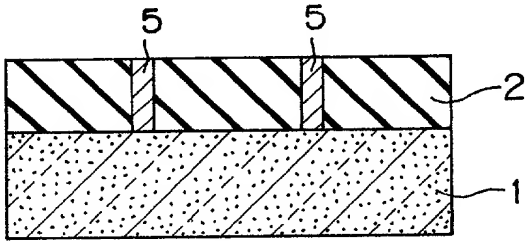


Fig.3E

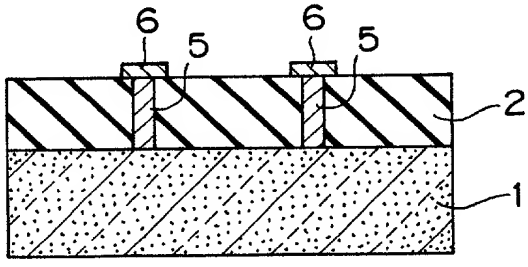


Fig.3F

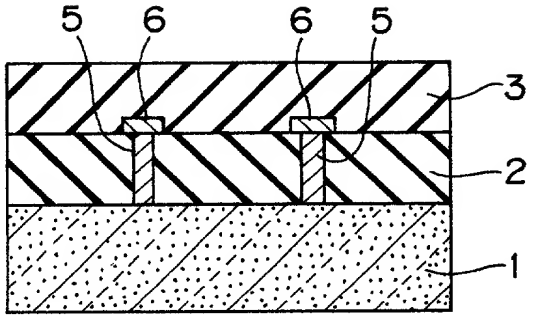


Fig.3G

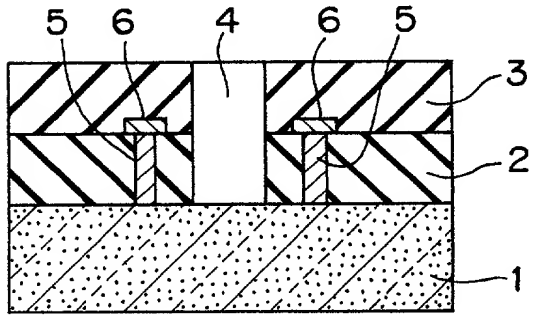


Fig.5A

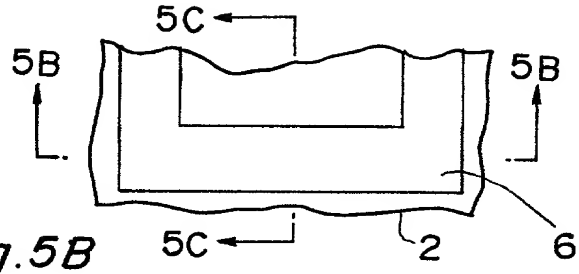


Fig.5C

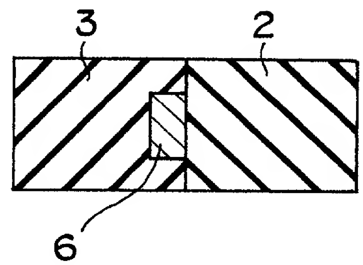


Fig.5B

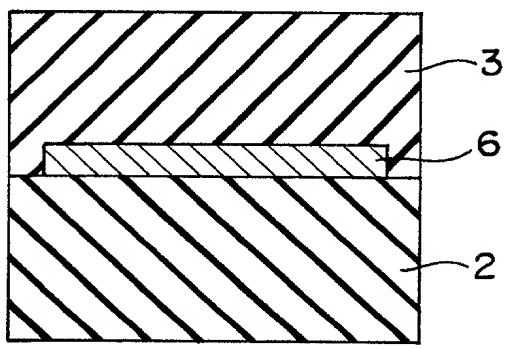


Fig.6A

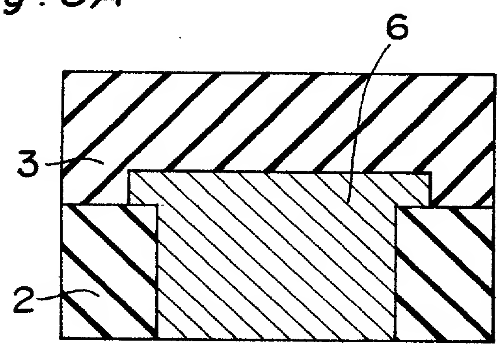


Fig.6B

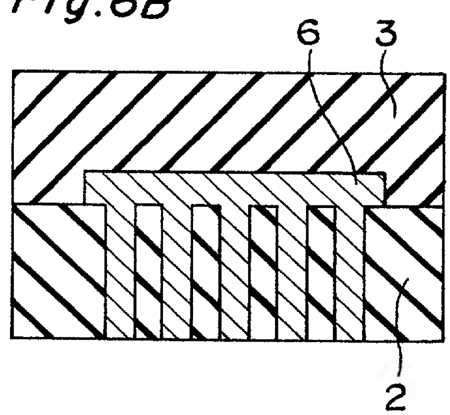


Fig.7

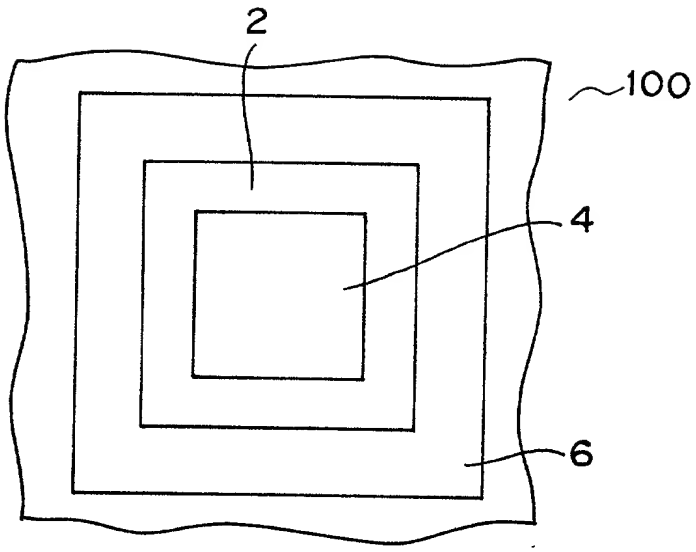


Fig.8

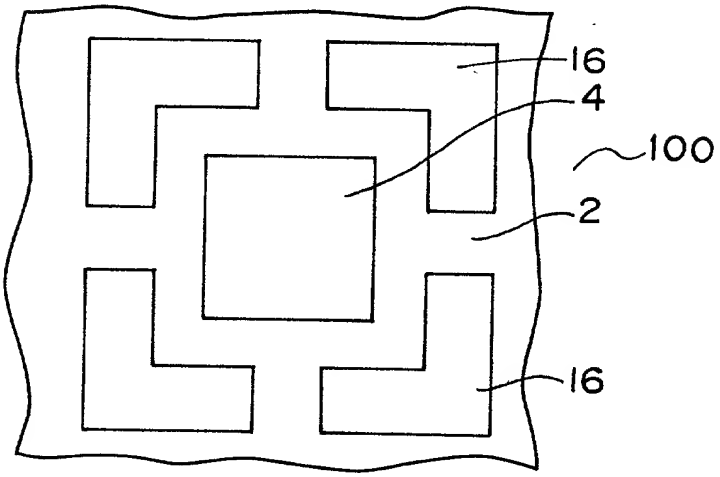


Fig.9

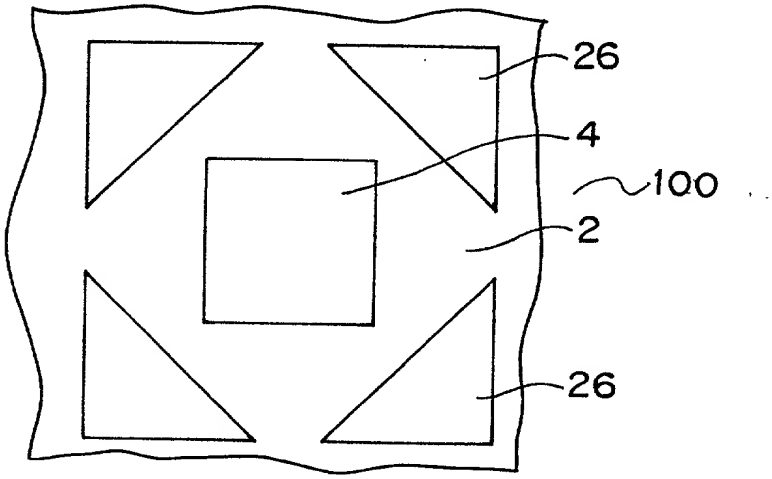


Fig.10

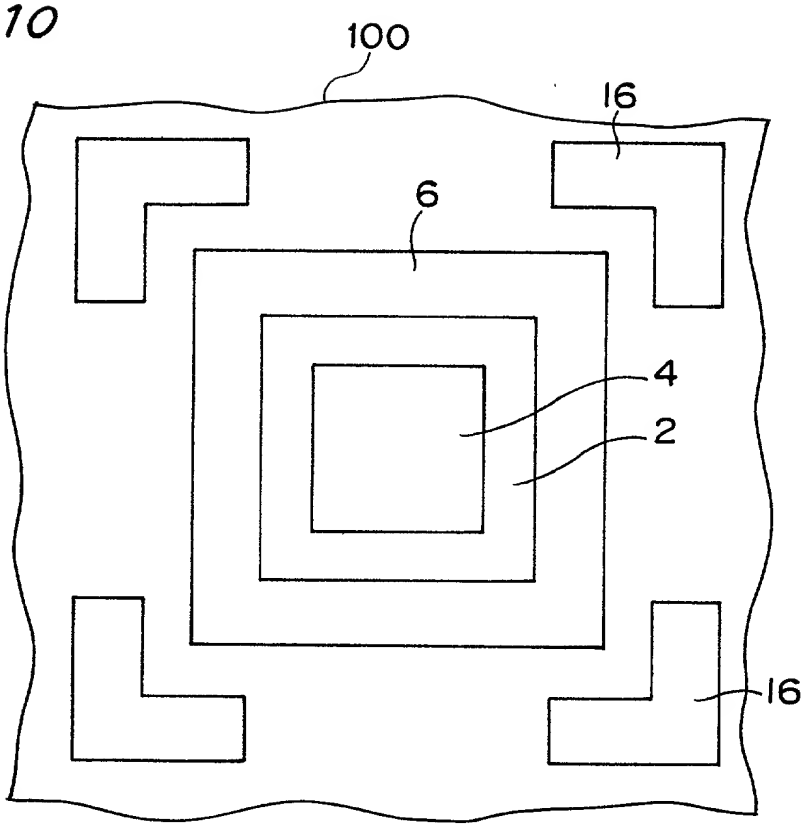


Fig.11

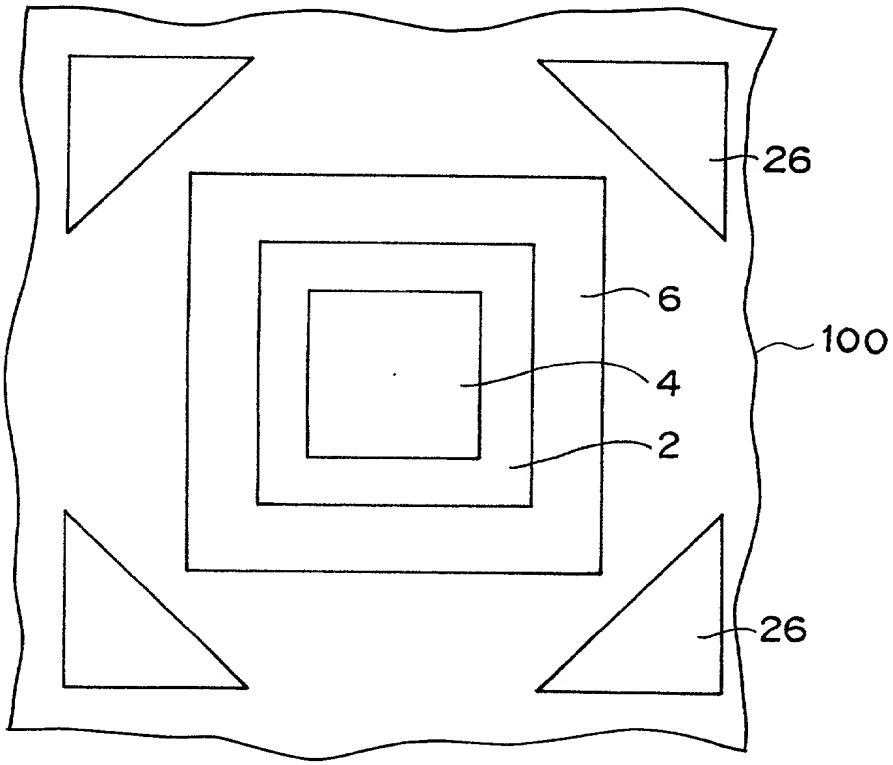


Fig. 12

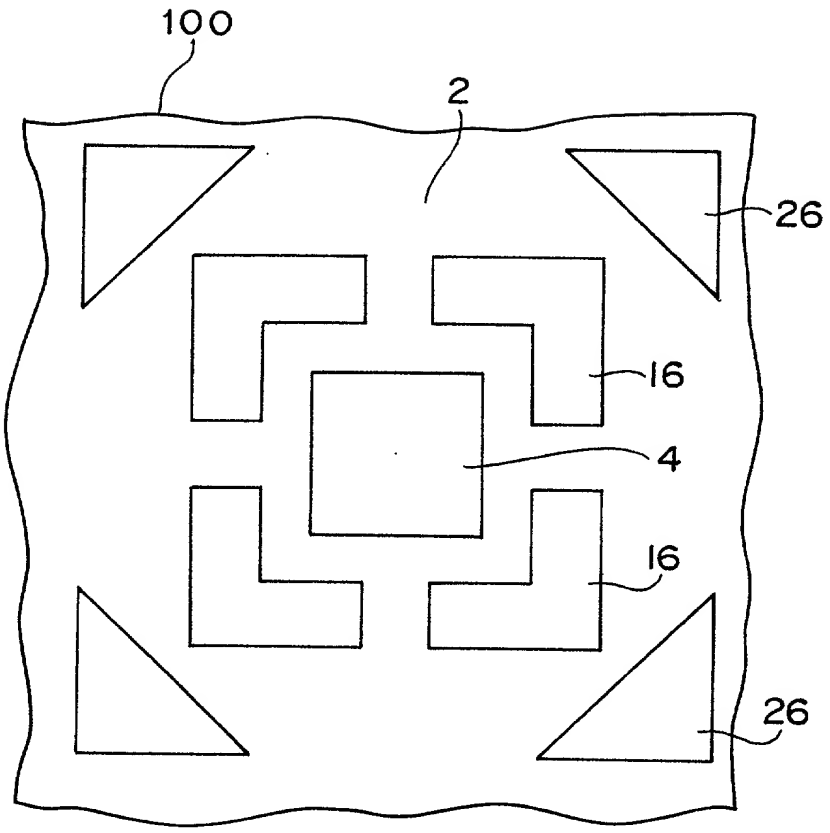


Fig.13A PRIOR ART

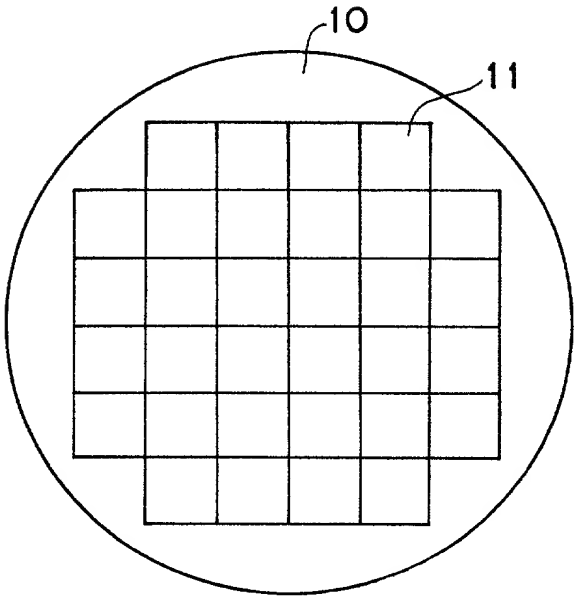


Fig.13B PRIOR ART

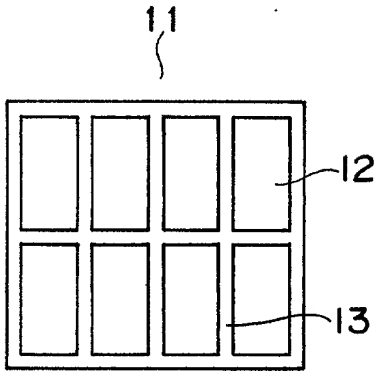


Fig.14A PRIOR ART

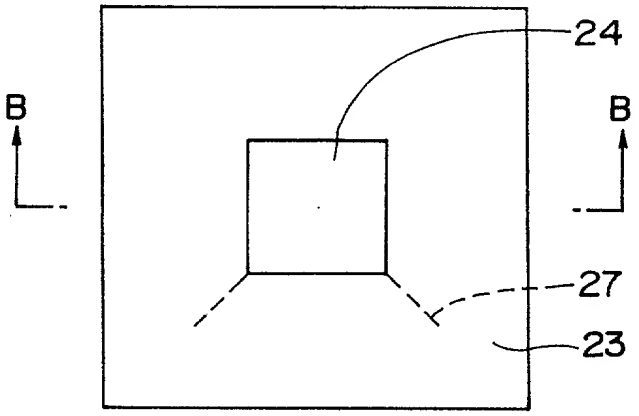


Fig.14B PRIOR ART

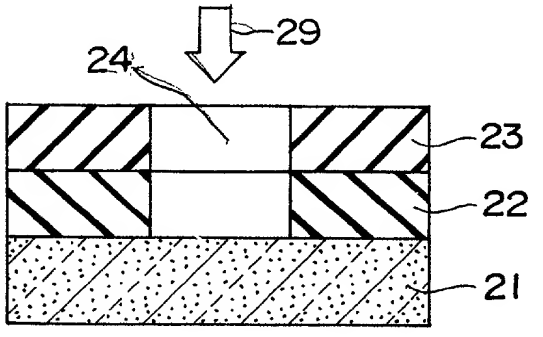


Fig.15A PRIOR ART

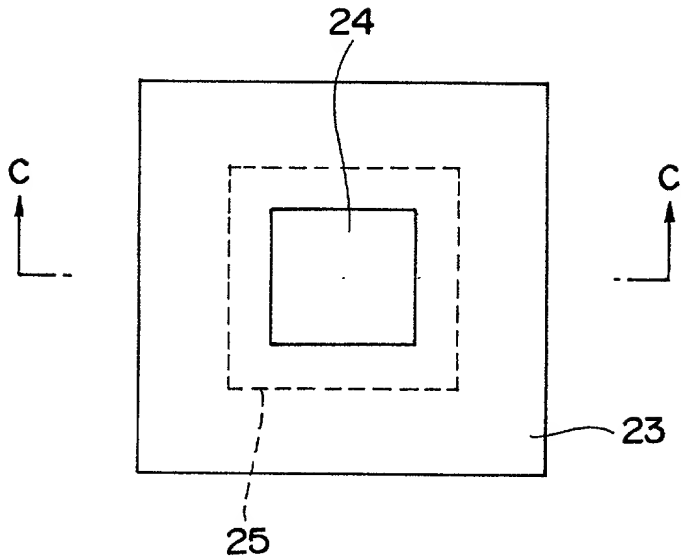
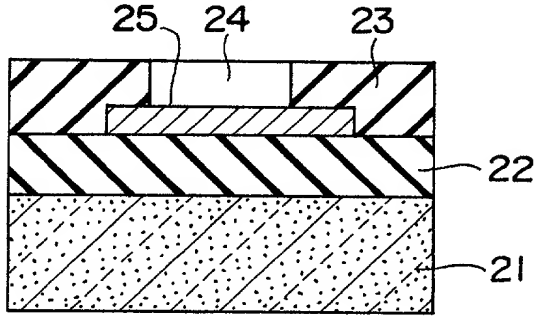


Fig.15B PRIOR ART



Attorney Docket No. _____

COMBINED DECLARATION/POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor(s), I(we) hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled SEMICONDUTOR DEVICE HAVING TEST MARK _____, the specification of which

(check one)

X is attached hereto.

___ was filed on _____ as United States Application No._____

___ PCT International Patent Application Number_____ filed _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed
2000-015760 (Number)	Japan (Country)	25/01/2000 (Day/Month/Year Filed)	X Yes ___ No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	___ Yes ___ No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	___ Yes ___ No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Appln. Serial No.)	(Filing Date)	(Status-patented, pending, abandoned)
(Appln. Serial No.)	(Filing Date)	(Status-patented, pending, abandoned)

I hereby appoint as my attorneys, with full power of substitution and revocation, to prosecute the patent application identified above and to transact all business in the U.S. Patent and Trademark Office connected therewith: Edward A. Becker, Reg. No. 37,777; Stephen A. Becker, Reg. No. 26,527; Marcel K. Bingham, Reg. No. 42,327; John G. Bisbikis, Reg. No. 37,095; Daniel Bucca, Reg. No. 42,368; Kenneth L. Cage, Reg. No. 26,151; Stephen C. Carlson, Reg. No. 39,929; Tom A. Corrado, Reg. No. 42,439; Paul Devinsky, Reg. No. 28,553; Laura A. Donnelly, Reg. No. 38,435; Margaret M. Duncan, Reg. No. 30,879; Brian E. Ferguson, Reg. No. 36,801; Michael F. Fogarty, Reg. No. 36,139; Willem F. Gadiano, Reg. No. 37,136; Keith E. George, Reg. No. 34,111; John A. Hankins, Reg. No. 32,029; Brian D. Hickman, Reg. No. 35,894; Eric J. Kraus, Reg. No. 36,190; Patrick B. Law, Reg. No. 41,549; Robert E. LeBlanc, Reg. No. 17,219; Jack Q. Lever, Reg. No. 28 ,149; Raphael V. Lupo, Reg. No. 28,363; Christine F. Martin, Reg. No. 39.762; Michael A. Messina, Reg. No. 33,424; Eugene J. Molinelli, Reg. No. 42,901; Christopher J. Palermo, Reg. No. 42,056; Joseph H. Paquin, Jr., Reg. No. 31,647; Robert L. Price, Reg. No. 22,685; Gene Z. Rubinson, Reg. No. 33,351; Joy Ann G. Serauskas, Reg. No. 27,952; David A. Spenard, Reg. No. 37,449; Arthur J. Steiner, Reg. No. 26,106; David L. Stewart, Reg. No. 37,578; Michael D. Switzer, Reg. No. 39,552; Leonid D. Thenor, Reg. No. 39,397; Keith J. Townsend, Reg. No. 40,358; Aaron Weisstuch, Reg. No. P41,557; Edward J. Wise, Reg. No. 34,523; Alexander V. Yampolsky, Reg. No. 36,324; and Robert W. Zelnick, Reg. No. 36,976 all of

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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